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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 08/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/529,621	BERENYI ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/30/2005 Preliminary Amendment*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-16,21,23 and 24* is/are rejected.

7)☒ Claim(s) *11,17-20 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "special purpose register" (claim 8 and 19) and "automatic transfer engines" (claims 7 and 17) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Note that element 301 is a memory access controller as claimed in 11.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

Claims 3, 6-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3, 7-9 are directed to an apparatus. However, the essential structural cooperative relationship(s) between the so-called "control and configure circuit," automatic transfer engines." "special purpose register" and other recited elements in the claims have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

MPEP 2172.01 requires that relationships between elements recited in the claims must be specified. Specifically, MPEP 2172.02 requires interrelation and structural relationships between essential elements in the claims. Therefore, it is the Examiner's position that the claimed elements, as defined in the originally filed specification and as identified above, are essential elements to the claimed invention. Since they are essential elements as defined in the originally filed specification, their structural cooperative relationships must be provided in the claims. Further, it is also the Examiner's position that the claimed elements, as identified above, function simultaneously, are directly functionally related, directly inter-cooperate, and/or serve independent purposes, as evidenced from the originally filed specification.

If Applicants disagree with the Examiner that the above identified elements, as defined by the originally filed specification, are essential elements to the claimed

invention, and that the above identified elements are directly functionally related, directly inter-cooperate, and/or serve independent purposes, it is requested that Applicants provide evidences showing that the identified elements are not essential elements to the claimed invention, do not function simultaneously, are not directly functionally related, do not directly inter-cooperate, and/or do not serve independent purposes; and state on the record that this is the case.

Further, it is unclear what may be the so-called "automatic transfer engines." It is unclear whether the "memory access controller" and the "automatic transfer engines" are the same means.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 10, 12-16, 21, and 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Foster et al. (6,038,630, Foster).

As broadly drafted and at best the Examiner can ascertain from the language of the claims, claims 1-5, 10, 12-16, 21, and 23-24 do not define any structure that differs from Foster.

With regard to claim 1, Foster discloses an electrical device for efficient and flexible control of memory access, the device comprising: at least two access channel circuits (defined by the dual path memory controller 230 as shown in Figs. 2 and 3; see column 4, line 4 to column 5, line 13. Note that as shown in Fig. 1, more than 2 channels can be employed), wherein at least one of the access channel circuits is connected to at least one memory accessing unit via at least one system bus and to at least one physical memory module, of a memory (the dual access channel as shown in Fig. 3 is connected to a processor 213, for example, via one of buses 1 and 2, Figs. 2 and 3, and to at least one physical memory module such as SDRAM or DRAM; see at least column 4, lines 14-34); the at least one access channel circuit providing memory access for the at least one memory accessing unit to at least a part of the memory (it is clear that at least one of the access channel circuits defined by one of the dual access channel controller 230 provides memory access for the at least processor 213 to at least a part of the memory; see at least column 4, lines 35-47).

With regard to claim 2, it is clear from at least Figs. 2 and 3 of Foster that functional units 1-N as shown in Fig. 1 including the processor 213, Fig. 2, define a plurality of memory accessing units (see at least column 3, line 52 to column 4, line 13), and wherein the at least two access channel circuits each provides memory access for at least one of the plurality of memory accessing units to at least a part of the memory

3, line 52 to column 4, line 34) thereby allowing the memory accessing units connected to different access channel circuits independent and simultaneous/parallel access to different parts of the memory (see at least column 3, line 52 to column 4, lines 65).

With regard to claim 3, the device further comprises: a control and configure circuit configured to dynamically control the at least two access channel circuits, the control and configure circuit allowing for an addition of additional access channel circuits (as shown in Figs. 2 and 3, the dual path memory controller 230 further defines a so-called "control and configure circuit " allowing the addition of additional channels. As shown in Fig. 1 more than 2 access channels or multi path access channel can be employed).

With regard to claim 4, it is clear that the at least one memory accessing unit comprises a plurality of memory accessing units (it is clear from at least Figs. 2 and 3 of Foster that functional units 1-N as shown in Fig. 1 including the processor 213, Fig. 2, define a plurality of memory accessing units; see at least column 3, line 52 to column 4, line 13), and wherein the at least two access channel circuits are each connected via the at least one system bus to one of the plurality of memory accessing units and each of the at least two access channel circuits are connected to receive information/data from at least a part of the memory (each of the dual access channel as shown in Fig. 3 is connected to each of the plurality of functional units 1-N including processor 213, and one additional unit shown in Fig. 2, for example, via at least one of buses 1 and 2, Figs. 2 and 3, to receive information/data from at least a part of one physical memory module such as SDRAM or DRAM; see at least column 4, lines 14-34).

With regard to claim 5, it is clear that the at least one memory accessing unit comprises a plurality of memory accessing units (it is clear from at least Figs. 2 and 3 of Foster that functional units 1-N as shown in Fig. 1 including the processor 213, Fig. 2, define a plurality of memory accessing units; see at least column 3, line 52 to column 4, line 13), and wherein the at least two access channel circuits are each connected via the at least one system bus to one of the plurality of memory accessing units and each of the at least two access channel circuits are connected to receive information/data from at least a part of the memory (each of the dual access channel as shown in Fig. 3 is connected to each of the plurality of functional units 1-N including processor 213, and one additional unit shown in Fig. 2, for example, via at least one of buses 1 and 2, Figs. 2 and 3, to receive information/data from and transmit information/data to at least a part of one physical memory module such as SDRAM or DRAM; see at least column 4, lines 14-34).

With regard to claim 10, it is clear from discussion above that the device has one access channel circuit for each connected memory accessing unit and wherein each access channel circuit is connected with each memory module of the memory.

With regard to claims 12-16, and 21, see discussion above, since the subject matter presented in these claims has already been addressed.

With regard to claims 23 and 24, since the device of Foster is audio related, it is clear that the device of Foster can be provided in a mobile communication terminal.

Claims 1-5, 10, 12-16, 21, and 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Welker et al. (Welker, 6,076,139).

As broadly drafted and at best the Examiner can ascertain from the language of the claims, claims1-5, 10, 12-16, 21, and 23-24 do not define any structure that differs from Welker.

With regard to claim 1, Welker discloses an electrical device for efficient and flexible control of memory access, the device comprising: at least two access channel circuits (any two of memory access channels 202-208 as shown in Figs. 2 and 3; see at least column 4, lines 1-11), wherein at least one of the access channel circuits is connected to at least one memory accessing unit via at least one system bus and to at least one physical memory module of a memory (at least one of the access channels 202-208 is connected to at least one of processing units 212-218, for example, via at least one system bus such as individual bus connecting to each of the processing units 212-218 and to at least one memory module RDRAM 210; see at least column 3, lines 30-67), the at least one access channel circuit providing memory access for the at least one memory accessing unit to at least a part of the memory (it is clear that the at least one access channel circuit 202-208 providing memory access for the at least one memory accessing unit 212-218 to at least a part of the memory RDRAM 210; see column 3, line 55 to column 4, line 67).

With regard to claim 2, the at least one memory accessing unit comprises a plurality of memory accessing units (212-218, Fig. 2, for example), and wherein the at least two access channel circuits (any two of 202-208) each provides memory access

for at least one of the plurality of memory accessing units (212-218) to at least a part of the memory (at least part of memory system 132) thereby allowing the memory accessing units (212-218) connected to different access channel circuits independent and simultaneous/parallel access to different parts of the memory (see at least the abstract, column 3, line 55 to column 4, line 67).

With regard to claim 3, the device further comprises: a control and configure circuit configured to dynamically control the at least two access channel circuits, the control and configure circuit allowing for an addition of additional access channel circuits (the memory interface 200 is readable as a so-called "control and configure circuit; see at least column 4, lines 31-67. One can configure the interface 200 to expand the number of channels).

With regard to claim 4, the at least one memory accessing unit comprises a plurality of memory accessing units, and wherein the at least two access channel circuits (202-208, for example; see at least column 4, lines 1-11) are each connected via the at least one system bus to one of the plurality of memory accessing units (see at least column 3, lines 30-67) and each of the at least two access channel circuits are connected to receive information/data from at least a part of the memory (it is clear that the at least one access channel circuit 202-208 providing memory access for the at least one memory accessing unit 212-218 to at least a part of the memory RDRAM 210; see column 3, line 55 to column 4, line 67).

With regard to claim 5, the at least one memory accessing unit comprises at least two memory accessing units (see at least column 3, lines 30-67), and wherein one of the at least two access channel circuits is connected via the at least one system bus to the at least two memory accessing units (202-208, for example; see at least column 4, lines 1-11), the one of the at least two access channel circuits being connected to receive data/information from and/or transmit data/information to at least a part of the memory (it is clear that the at least one access channel circuit 202-208 providing memory access for the at least one memory accessing unit 212-218 to at least a part of the memory RDRAM 210; see column 3, line 55 to column 4, line 67).

With regard to claims 12-16, and 21, see discussion above, since the subject matter presented in these claims has already been addressed.

With regard to claims 23 and 24, since the device of Foster is multi-media related, it is clear that the device of Foster can be provided in a mobile communication terminal.

Allowable Subject Matter

Claims 6-9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 11, 17-20, and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relevant Art

US Patent Nos. 6,378,049 to Stracovsky et al., 5,202,973 to Ramanujan et al., and 5,878,240 to Tomko are cited as relevant art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh Dang
Primary Examiner